**Synchronous FIFO Test Plan**

| **Test ID** | **Test Scenario** | **Objective** | **Expected Result** |
| --- | --- | --- | --- |
| T01 | Basic Write | Write a single data item into FIFO | Data is stored; full signal remains low |
| T02 | Basic Read | Read a single data item after write | Same data is read; empty signal remains low |
| T03 | Full Condition | Fill FIFO to max depth | full signal goes high; no further write allowed |
| T04 | Empty Condition | Read all items until FIFO is empty | empty signal goes high; no further read allowed |
| T05 | Simultaneous Read/Write | Perform read and write in same clock cycle | FIFO maintains data ordering; no corruption |
| T06 | Overflow Attempt | Attempt to write when FIFO is full | Write is ignored; FIFO stays full |
| T07 | Underflow Attempt | Attempt to read when FIFO is empty | Read is ignored; FIFO stays empty |
| T08 | Pointer Wraparound | Write and read continuously over depth + cycles | FIFO handles wraparound correctly |
| T09 | Reset Behavior | Apply asynchronous reset during operation | FIFO clears data; pointers reset; flags reset |
| T10 | Back-to-Back Operations | Continuous write/read without delay | No data loss; FIFO performance validated |
| T11 | Randomized Access Pattern | Random rd\_en/wr\_en with constrained data | FIFO maintains FIFO ordering; coverage points hit |
| T12 | Status Flag Verification | Validate full/empty flags at boundaries | Flags assert/deassert as expected |
| T13 | Latency Check | Measure delay from write to read | Latency matches depth/flow expectations |
| T14 | Data Integrity | Compare written and read data using scoreboard | All output matches expected input values |
| T15 | Sequence Stress Test | Run long sequence with burst traffic | FIFO remains stable without loss or corruption |